A Research Paper on Power Optimization of MUX Module

Sharayu Amol Shinde[1], Dr.M.S.Kumbhar[2]

[1]Student, Rajarambapu Institute of Technology(India), affiliated to Shivaji University, sharayu96@gmail.com

[2]Proffesor, Rajarambapu Institute of Technology(India), affiliated to Shivaji University, mahesh.kumbhar@ritinia.edu

ABSTRACT

This file High speed, low power and less area are the basic needs for any of the digital circuits. In today's world, low power has come out as a principal concept of electronics world. Power optimization has become a key point for the area and performance of VLSI Chip design. With a shrinking technology, over all power management and power optimization are the emerging challenges due to the increased complexity. For many VLSI designs, optimization of power is as important as timing due to the need to extend the battery life and reduce the cost**.** The design component has conflicting affect on overall performance of circuits. An optimization of power consumption can be achieved by altering different components and parameters of the circuit.

As far as digital circuits concerned, multiplexer is the basic circuitry of any digital circuit. The aim of this paper is to optimize power consumption of a multiplexer module. In this paper, the need of power optimization, techniques of power optimization and the techniques used to optimize the multiplexer modules are discussed. The multiplexer modules are designed in different logic styles and finally this paper has come up with an optimized multiplexer module. Along with the use of different logic styles, one of the parameters i.e. W/L ratio of MOSFET which affects the power consumption is also altered so as to reach the optimum results.

Keywords*:* Multiplexer, VLSI (Very Large Scale Integration),power optimization, Tanner EDA

1. INTRODUCTION

The increasing complexity and speed of today's designs leads to a significant increase in the power consumption of very-large-scale integration (VLSI) circuits. To meet this requirement, various techniques of designing the circuit and parameters of transistors like power dissipation, switching capacitance, transition activity, and short-circuit currents are being worked upon to reduce power. The power consumption strongly depends upon the logic style used to design the circuit.[21] Depending upon the kind of circuit to be implemented, its application and the design techniques and methodologies used, various performance aspects come into the picture, denying the formation of universal rules for optimal logic styles.

In this paper, 2:1 multiplexer is implemented using CMOS, CMOS transmission gate logic, Pass transistor logic styles and NMOS pass transistor logic. A low power multiplexer is developed referring to the above mentioned logic styles which consume less power compared to the multiplexers designed using those logic styles.

A multiplexer is a device that selects one of many input signals and forwards that particular selected input its output. A multiplexer of n select lines (which selects which input line has to be sent to the output) has 2^n inputs and one output and hence it is also called a data selector. Multiplexer being a basic circuit can be used to implement any combinational circuit. So by optimizing design of multiplexer, many combinational circuits can be power optimized. Below figures show the block diagram and truth table for 2:1 multiplexer given below.

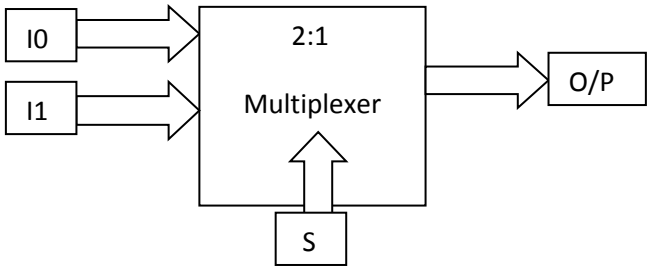

Figure 1.1 2:1 MUX

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Table.1.1 Truth table for 2to1 multiplexer

S	OUT
0	I0
1	I1

2. Power Consumption Concepts

2.1 Power Management

Power consumption concern comes into the picture when the portable electronic systems started coming up. In these systems, the battery lifetime is a necessary element for the commercial success of the product[5]. A high absolute level of power is not just undesirable, but also it leads to heat dissipation. Thus to keep the system in a working condition at acceptable temperatures, systems may require heat removal system in turn adding to the circuitry and cost of the systems. Hence power management plays a key role in almost every aspect of an electronic system.

2.2 Benefits of Power Optimization

Power consumption provides many benefits such as less heat is generated, which overcome many problems associated with high temperature, such as the need for heat sinks. This in turn provides low cost product to the consumer. As heat dissipation is reduced, the reliability of the system is increased due to lower temperature stress gradients on the device[15]. The extended life of the battery in battery-powered systems is achieved.

2.3 Sources of Power Consumption

There are primarily three main causes of power dissipation in the digital circuits:

A] Static Power Dissipation
B] Dynamic Power Dissipation
C] Short-Circuit Power Dissipation

A] Static Power Dissipation

The static power components come into play when the circuits are at rest, i.e. when there is no supply to ye circuit or they are biased to a specific state or there is no activity in the circuits. The static power dissipation consists of reversed-biased diode leakage and sub threshold currents. Because of necessity of down-scaling of threshold voltages, the sub threshold leakage becomes more and more pronounced[21]. In weak inversion, below the threshold voltage, the transistors do not turn completely off. The sub threshold current depends on the threshold voltage. Dynamic power is only when there is switching but static power is permanent[9].

$$P_s = I_{leakage} * V_{dd} \qquad \text{Eqn 2.3.a}$$

where,

$I_{leakage}$: Leakage current

V_{dd}: Supply Voltage

B] Dynamic Power Dissipation

Dynamic power dissipation depends on the activity, timing, output capacitance, and supply voltage of the circuit. The repeated charging and discharging of the output capacitance is necessary to transmit information in CMOS circuits.This charging and discharging of the node capacitances causes for the switched power dissipation[25].

$$P_{dyn} = C_L . V_{dd}^{\,2} . f \qquad \text{Eqn 2.3.b}$$

where,

C_L: Load Capacitance

V_{dd}: Supply Voltage

f : frequency of the input signal

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C] Short Circuit Power Dissipation

In real time circuit operations, signals have non-zero rise and fall times which causes both the P and N networks of the CMOS circuit to conduct simultaneously i.e. both nmos and pmos transistors may conduct simultaneously for short amount of time during switching. This current is called short circuit current consumption and it does not contribute to the charging/discharging of the capacitance in the circuit. This component is especially prevalent if the input signal rise time and fall times are large or/and the output load capacitance is small[29].

$$P_{sc} = I_{mean} * V_{dd} \qquad \text{Eqn2.3.c}$$

where,

I_{mean} = average current

V_{dd} = Supply Voltage

2. 4 Optimization Techniques in VLSI

The power optimization in VLSI is mainly done by the following techniques

- Transistor sizing: In this technique the size (width and length) of each gate is altered for minimum power usage. Transistor sizing in a combinational gate circuit has pronounced effect on power dissipation and circuit delay[11]. As the size of the transistors in a given gate increases, the delay of the transistor decreases, but the power dissipated increases.

- Power gating: High threshold voltage sleep transistors are used in this technique. They cut-off a circuit block when the block is not in dynamic state i.e. it is not switching. An important design parameter is sleep transistor sizing. This helps reducing the stand-by or leakage power[14].

- Logic styles: Using different types of logics such as cmos logic, transmission gate logic, pass transistor logic, pseudo nmos logic, etc. According to the requirement of the applications, various logics can be implemented based on speed, area, power.

- Voltage scaling: Voltage at which the component works is increased or decreased without affecting the end result of the circuit[27]. Voltage scaling is again divided into three categories static voltage scaling, dynamic voltage scaling and adaptive voltage scaling. Though lower supply voltages use less power, the delay increases.

- Voltage islands: Separate blocks are run at different voltage levels for saving power. Level-shifters are used so that when two blocks with different supply voltages are present, they communicate with each other through it.

- Variable VDD: The supple voltage of a single block is varied during operation, high voltage (and high power) when the block needs to go fast and low voltage when slow operation is acceptable.

- Multiple threshold voltages: Latest techniques can help build transistors with varying threshold voltages. Combination with number of different threshold voltages of CMOS transistors can save power[17].

3. Methods Adopted for Power Optimization

3.1 Logic Styles Used For MUX Modules

In this paper, MUX modules are first designed conventionally using the logic styles like CMOS logic, NMOS Pass Transistor Logic, Pass Transistor Logic and Transmission gate Logic. Towards the end of this section, optimized MUX module is being discussed.

A] CMOS Logic Style

The fundamental building blocks of CMOS circuits are P-type and N-type MOSFET transistors. A P-type MOSFET can be modeled as a switch that is closed when the input voltage is low (0 V) and open when the input voltage is high (5 V). A N-type MOSFET can be modeled as a switch that is closed when the input voltage is high (5 V) and open when the input voltage is low (0 V). The basic idea for CMOS technology is to combine P-type and N-type MOSFETs such that there is never a conducting path from the supply voltage (5 V) to ground[13]. As a

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consequence, CMOS circuits consume very little energy. The symbol for an n-channel transistor and p- channel transistor are shown in figure below.

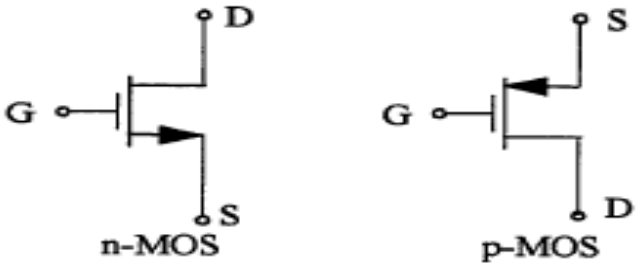

Fig. 3.1.a NMOS Transistor Fig.3.1.b PMOS Transistor

B] Pass Transistor Logic and NMOS Pass Transistor Logic

In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors[6]. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input[16]. Pass transistor logic often uses fewer transistors, runs faster, and requires less power than the same function implemented with the same transistors in fully complementary CMOS logic.

C] NMOS-Pass Transistor:

The gate of both the transistors is static. A low-impedance path exists to both supply rails under all circumstances. N numbers of transistors are required instead of 2N that in CMOS logic style. Power consumption is less compared to that of the CMOS logic style[3]. In this logic style, the transistors work bidirectionally (versus that in CMOS logic style which is unidirectional).

There are two types of pass transistors:

i. NMOS Pass: Passes strong logic '1' and weak logic '0'

ii.PMOS Pass: Passes strong logic '0' and weak logic '1'

D] Transmission Gate Logic

The Transmission Gate, (TG) is a bilateral switch, which is not possible with a single MOS device. TGL can have either of its terminals can be the input or the output. As well as the input and output terminals, the transmission gate has a third connection called the control, where the control input determines the switching state of the gate as an open or closed (NO/NC) switch. The advantage of using both in an arranged network is that the P-type MOSFET passes strong logic 1 and weak logic 0 and P-type MOSFET passes strong logic 0 and weak logic 1[12]. Hence we get both i.e. strong logic 1 and logic 0.Therefore, connecting an NMOS transistor with a PMOS transistor in parallel provides a single bilateral switch which offers efficient output drive capability for CMOS logic gates controlled by a single input logic level. The symbol of TGL is given below.

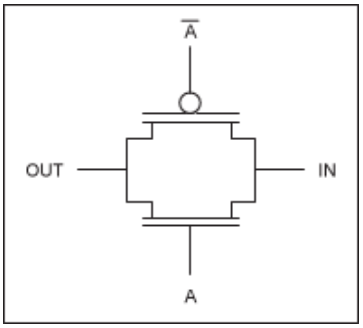

Fig. 3.1.c Transmission Gate Logic Transistor

E] Optimized Module

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The optimized MUX module is designed using the CMOS logic style with the addition of a PMOS connected at the bottom end of the CMOS MUX module as a pull-down sleep transistor and the output drives its gate. The optimized module works similarly to that of the conventional CMOS module. But the difference is the output is obtained only if the value of the output is high (logic 1) therefore supplying the gate of PMOS sleep transistor with a high logic. This high logic turns the PMOS off and hence the output is obtained as it is. Otherwise the whole circuit remains off irrespective of the input. This means that the circuit remains off for any low input and turns on only if output is high.

This ensures that the circuit remains in off state except for when the output is high thus lowering the power consumption by the circuit. The circuit consumes power only when the output is high. The truth table for optimized 2:1 MUX module is given as follows:

Table3.1.a. Truth Table of Optimized MUX Module

S	Input	OUT
0	I0= 0	0
	I0= 1	1
1	I1=0	0
	I1=1	1

3.2 Power Analysis

To calculate the power theoretically, the following given formulae were used:

1. Gate capacitance

$$C_G = W.L.C_{OX} \quad \text{Eqn 3.2.a}$$

2. Diffusion capacitances

$$C_{diff} = Cj \cdot L \cdot W + Cjsw \cdot (2L+W) + Cjgate \cdot W \quad \text{Eqn 3.2.b}$$

3. Gate Overlap Capacitance

$$C_o = C_{OX} \cdot x_d \quad \text{Eqn 3.2.c}$$

where,

W= width of gate

L= length of gate

C_{OX} = Capacitance of oxide layer

Cj= Junction Capacitance

Cjsw= Side wall Junction Capacitance

Cjgate=Gate Junction Capacitance

x_d= thickness of gate and drain/source layers

Load Capacitance is given as:

$$C_L = C_G + C_{diff} + C_o \quad \text{Eqn 3.2.c}$$

The power results are obtained by simulation of the MUX Modules on Tanner EDA Tool on 250nm of technology. The results of simulation are displayed in the Results section.

4. Results

The power consumed by all types of MUX modules is analyzed by both theoretical as well as simulation method.

Theoretical Analysis

The power of each MUX module is calculated by using the following mathematical formulae:

i. $P_{dyn} = C_L . V_{dd}^2 . f$ from **Eqn2.3.2**

ii. $C_L = C_G + C_{diff} + C_o$ from **Eqn 3.2.c**

iii. $C_G = W.L.C_{OX}$ from **Eqn 3.2.a**

iv. $C_{diff} = Cj \cdot L \cdot W + Cjsw \cdot (2L+W) + Cjgate \cdot W$ from **Eqn 3.2.b**

v. $C_o = C_{OX} \cdot x_d$ from **Eqn 3.2.c**

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By calculating the above mentioned capacitances we dynamic power mentioned in table 4.1.

Following are the schematics and output waveforms of the simulated MUX Modules.

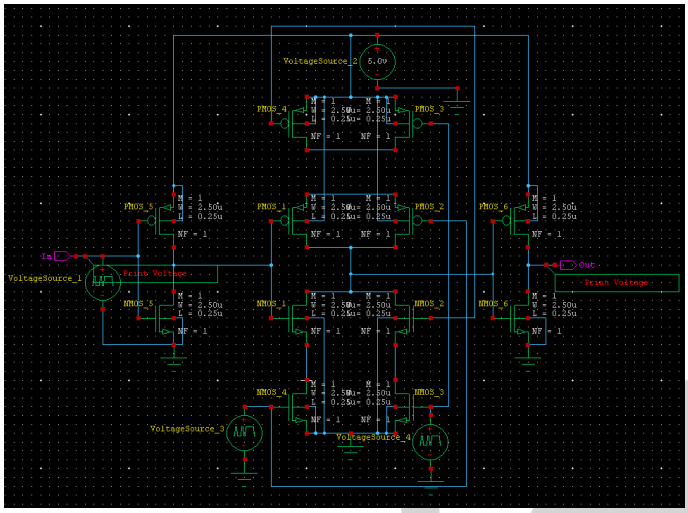


Figure 5.1a Schematic of CMOS MUX

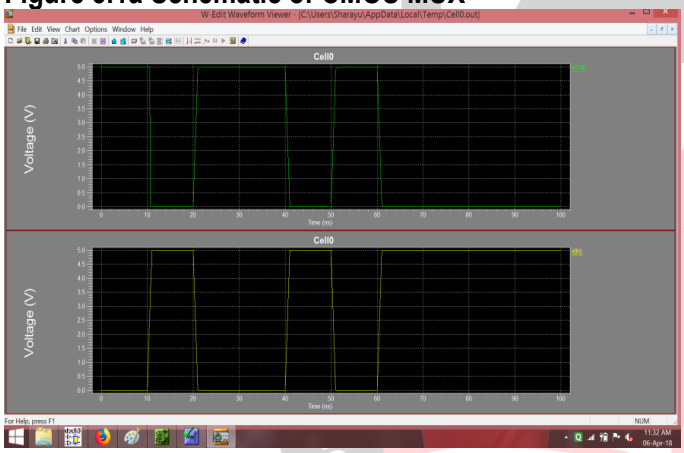


Figure 5.1b Output Waveforms of CMOS MUX

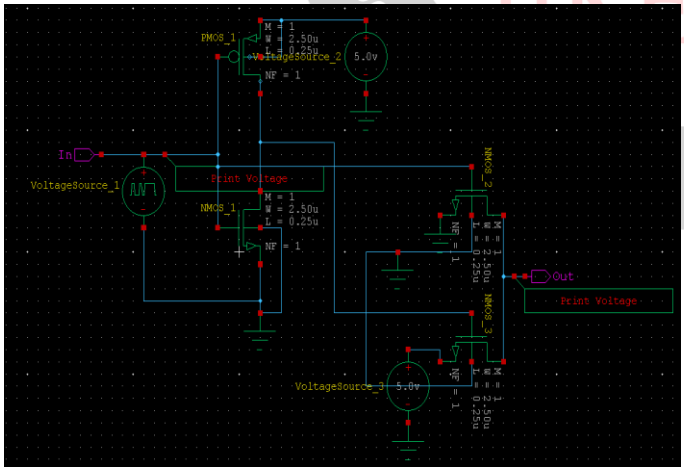
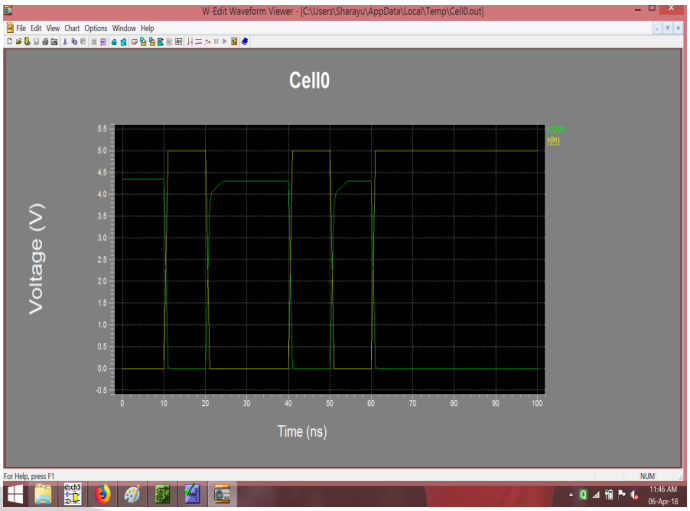


Figure 5.2a Schematic of NMOS MUX



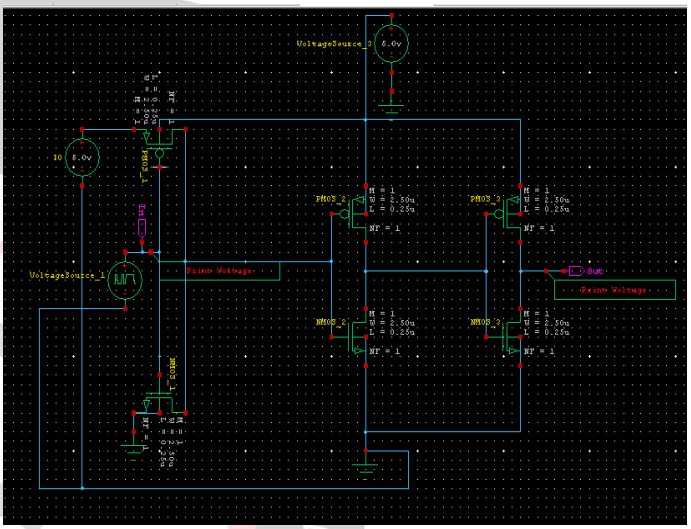


Figure 5.3a Schematic of Pass Transistor MUX

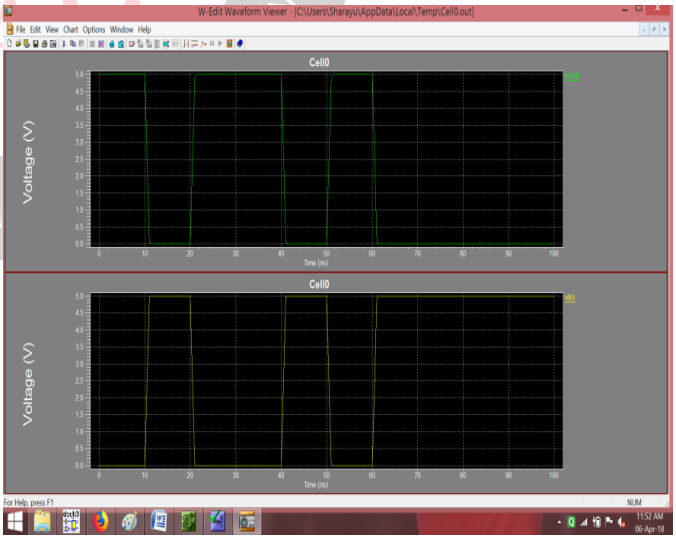


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Figure 5.3b Output Waveforms of Pass Transistor MUX

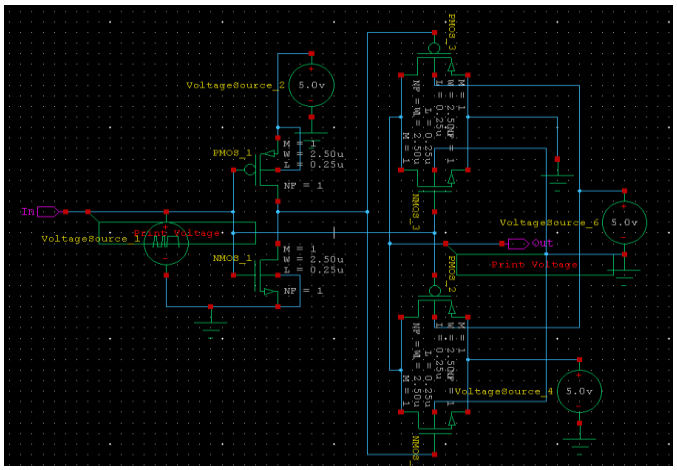

Figure 5.3a Schematic of Pass Transistor MUX

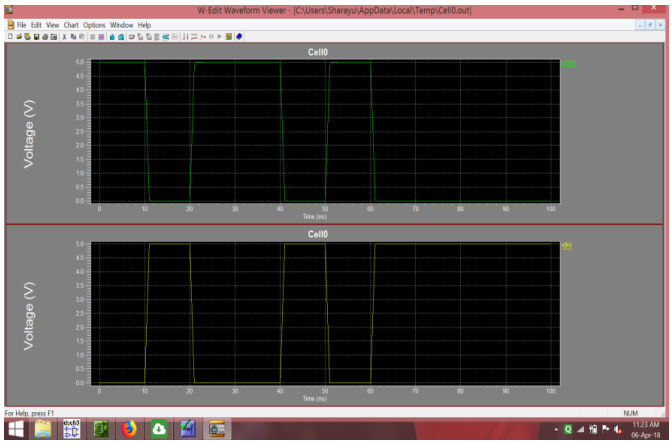

Figure 5.4b Output Waveforms of TGL NMOS MUX

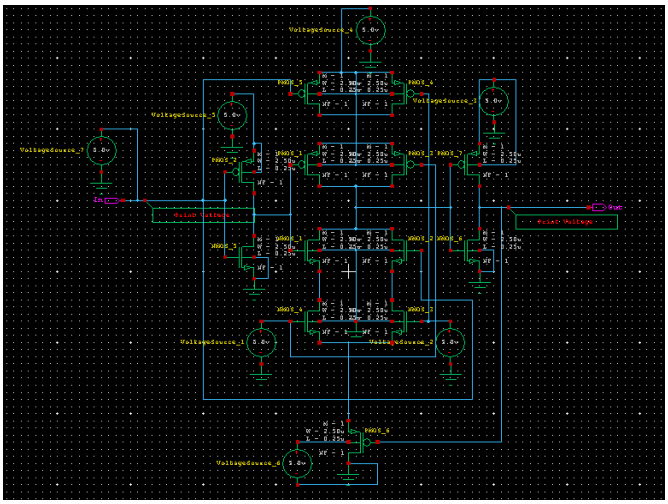

Figure 5.5a Schematic of Optimized MUX

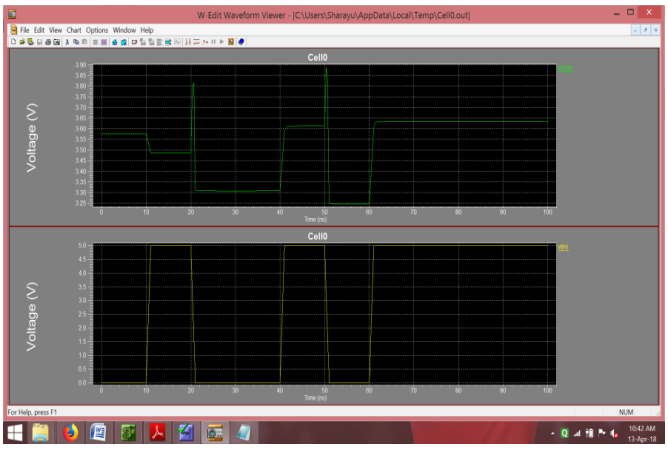

Figure 5.5b Output Waveforms of Optimized MUX

Here are the results obtained by simulation done on Tanner EDA on 250nm of technology.

Table 4.1 Power Results

Sr.No	Logic Style	Power simulated (W)	Power calculated (W)
1.	CMOS	5.980564e-006	6.75-006
2.	NMOS	7.572388e-006	11.25e-006
3.	PTL	1.188082e-006	3.28e-006
4.	TGL	2.553231e-006	3.73e-006
5.	OPT	7.565226e-009	2.03e-006

5. Conclusion

In this paper the challenge of power optimization of 2:1 MUX module on 250nm technology was taken up and resolved. After studying various methods and techniques for power optimization, one way that is developing MUX module using different logic styles was finalized and worked upon. The optimized module of MUX developed on 250nm consumes the minimum power amongst all the other modules. Further, the optimized MUX module can be optimized by altering various parameters like W/L ratio, threshold voltages, etc according to the need of the application.

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