Design and Analysis of 20 nm T-Gate AlN/GaN HEMT with InGaN back-barrier for High power Microwave Applications

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ABSTRACT

This research article reports DC and microwave performance of ultra-scaled AlN/GaN/InGaN double heterojunction high electron mobility transistor (HEMT) on SiC substrate. The device structure is simulated by using Synopsys Sentaurus TCAD Drift-Diffusion transport model at room temperature. The device featuring n+ InGaN/GaN ohmic contacts, fully passivated device structure,and T-gate structure. Record current gain cut-off frequency (f_t) of 451 GHz and simultaneous power gain cut-off frequency (f_{max}) of 448 GHz were obtained for 20 nm gate length HEMT. Three terminal off-state breakdown voltage of 21 V and Johnson Figure of Merit (JFoM) of 9.4 THz-V were achieved by suppressing the leakage currents as well as parasitic delay. The short channel effects (SCEs) of the device is majorly reduced as SS = 81 mV/dec and DIBL = 112 mV/V. The preeminent microwave characteristics with the higher breakdown voltage of the proposed GaN-based HEMT are the expected to be the most optimistic applicant for future high power millimeter wave applications.

Keywords - HEMT, cut-off frequency, breakdown voltage, JFoM, short channel effects and back-barrier.

1. INTRODUCTION

The unique properties of both high electric breakdown field (~3.3 MV/cm) and high electron velocity (~2.5 × 10^7 cm/s) of the GaN based HEMT; it has been captivated for high power switching and high power RF applications [1]. In spite of tremendous research progresses has been made during the recent years, there are still several important issues that need to be overcome for further improving the cut-off frequency of GaN based HEMT in sub-millimeter region. For high gain millimeter wave power amplification, one of the key challenges is to increase the power gain cut-off frequency (f_{max}). f_{max} is the maximum frequency at which the transistor still provide the power gain and can be expressed as:

$$f_{max} = \frac{f_T}{2\sqrt{(R_i+R_s+R_g)/R_{ds} + (2\pi f_T)R_g C_{gd}}} \quad (1)$$

Where f_T is the current gain cut-off frequency and C_{gd} is the gate to drain capacitance, while R_i, R_s, R_g and R_{ds} represents gate charging, source, gate and output resistance, respectively. To increase the f_{max} each parameter need to be carefully optimized. In this article, we describe the new design features to reduce the parasitic components to achieve a very high f_{max}.

To lift-off the cut-off frequency of GaN-based microwave transistors, several technologies are adopted [2-18], such as innovative barrier materials (InAlN and AlN), gate engineering (recessed gate, T-gate and two fingered gate), n+ source/drain region (to minimize the contact resistances), surface passivation (SiN, Al_2O_3), different back-barrier (AlGaN and InGaN) and different scaling styles (vertical, lateral scaling & symmetric and asymmetric gate position). For high power RF and mixed-signal monolithic microwave integrated circuits (MMIC) applications, Johnson figure of merit (JFoM = $f_t \times V_{BR}$), power gain cut-off frequency (f_{max}) and drain current density (I_{ds}) and the breakdown voltage (V_{BR}) are the essential key parameters. The higher cut-off frequency is obtained by appropriate scaling of gate length and device design. However, the associated breakdown voltage (V_{BR}) of the device deteriorates as the device is scaling down. The lower breakdown voltage of the HEMTs limits the dynamic range of the device operation. On the other hand, the low aspect ratio Lg/d<5 (gate length to gate-channel separation) of lateral-scaled devices causes short channel effects (negative threshold voltage shift and increased DIBL). To suppress the short channel effects (SCEs), while maintaining thin barrier layer thickness alternate barrier material is needed for maintaining high 2DEG density and breakdown voltage (V_{BR}) simultaneously. During the last few years, InAlN and AlN material are used as the top barrier for the ultra-scaled device to achieve a high 2DEG density (>10^{13} cm^{-2}) with a smaller thickness without the need of modulation doping and also it greatly mitigates the gate leakage current with the help of large barrier height. To enhance both the f_t and f_{max} with high breakdown voltage simultaneously, proper device design and

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scaling are required. For achieving high f_t and f_{max}, the critical key parameters such as gate-drain capacitance (C_{gd}), drain conductance (g_d), contact resistances (R_s & R_d), device on-resistance (R_{on}) and gate resistance (R_g) of the transistor are to be minimized.

Dong Seup Lee et al. (2011) designed 30nm gate length InAlN/GaN HEMT with oxygen plasma treatment, and the HEMT exhibited a f_t/f_{max} of 245/13 GHz [2] . Stefano Tirelli et al. (2011) demonstrated a peak f_t/f_{max} of 205/220 GHz for 30nm InAlN/GaN HEMT with fully passivate ddevice surface [3] . Ronghua Wang et al. (2010) reported f_t/f_{max} of 70/105 GHz, V_{BR} of 29 V for 150 nm gate length enhancement mode InAlN/GaN HEMT [4] . Yuanzheng Yue et al. (2012) had shown the record f_t of 370 GHz for 30 nm InAlN/GaN HEMT, however the f_{max} of the transistor is 28 GHz and severe short channel effects were found [5] . Chuan-Wei Tsou et al. (2015) demonstrated f_t/f_{max} of 60/101 GHz, 21 V breakdown voltage for 110 nm InAlN/GaN on Si substrate [6].

From the aforementioned literature research, for ultra-scaled (sub 50 nm gate lengths) InAlN/GaN HEMTs are failed to attain high breakdown voltage. However, the important figure of merit of GaN-based transistors is high breakdown voltage.

Sheng Lei Zhao et al. (2016) investigated the breakdown voltage of AlGaN/HEMT with AlGaN back-barrier [7]. The HEMT with AlGaN back-barrier manifested a high breakdown voltage than conventional HEMT by suppressing the buffer leakage currents. Hyung-Seok Lee et al. (2012) experimentally verified the breakdown voltage enhancement of InAlN/GaN HEMT by using AlGaN back-barrier [8].

Palacios et.al. demonstrated a f_t/f_{max} of 124/230 GHz for 100 nm gate length AlGaN/GaN HEMT with InGaN back-barrier [9].The InGaN back-barrier enhanced the electron confinement in 2DEG channel region. The N-polar GaN/AlN MISHEMT with 150 nm T-gate device manifested a f_t/f_{max} of 47/81 GHz [10] . Nidhi. et.al. displayed a f_t/f_{max} of 93/127 for 20 nm T-gate N-polar GaN-based MISHEMT [11] . Wang. et.al. demonstrated f_t/f_{max} of 70/105 with V_{BR} of 29V for 150 nm recessed T-gate InAlN/AlN/GaN HEMT and also the device had shown the suppressed SCEs [12] . 80 nm T-gate InAlN/AlN/GaN MISHEMT characteristics is demonstrated by Brian et al. the device exhibited a 95 V breakdown voltage and f_t/f_{max} of 114/230 GHz [13]. Chuan-wei et.al. designed 110 nm T-gate InAlN/GaN HEMT and demonstrated a f_t/f_{max} of 60/101 GHz while maintaining the breakdown voltage 21 V [14] . Eblabla et.al. demonstrated 300 nm two finger T-gate length AlGaN/AlN/GaN HEMT device characteristics and f_t/f_{max} of 55/121 GHz is achieved on Si substrate [15] . Han Tingting et.al demonstrated a f_t/f_{max} of 162/176 GHz for 70 nm T-gate InAlN/GaN on SiC substrate recently [16]. Despite the demonstration of f_t/f_{max} of the GaN based HEMTs from the literature research for different HEMT structure, the device leakage currents, SCEs and breakdown voltages are not come in to picture in many of the research work.

In this article, we proposed and demonstrated the DC and microwave characteristics of an ultra-scaled novel 20 nm D-mode T-gate AlN/GaN HEMT with InGaN back- barrier. The higher mobility and sheet charge density of AlN/GaN hetero junction have proven experimentally in [17] . A very thin 3.5 nm AlN barrier material is used as a top barrier in our work. The other features of the device are heavily doped n++ InGaN/GaN source and drain region effectively reduces the contact resistances [18], Al_2O_3 passivated device surface to lift-off the RF performance of the device by suppressing the C_{gd}, 2.5 nm GaN cap layer to mitigate the gate leakage current, T-shaped gate which minimizes R_g and InGaN back-barrier which helped the device for better confinement of carrier in channel and to avoid the buffer leakage current.

2. AlN/GaN HEMT WITH InGaN BACK-BARRIER DEVICE STRUCTURE AND BAND GAP DIAGRAM.

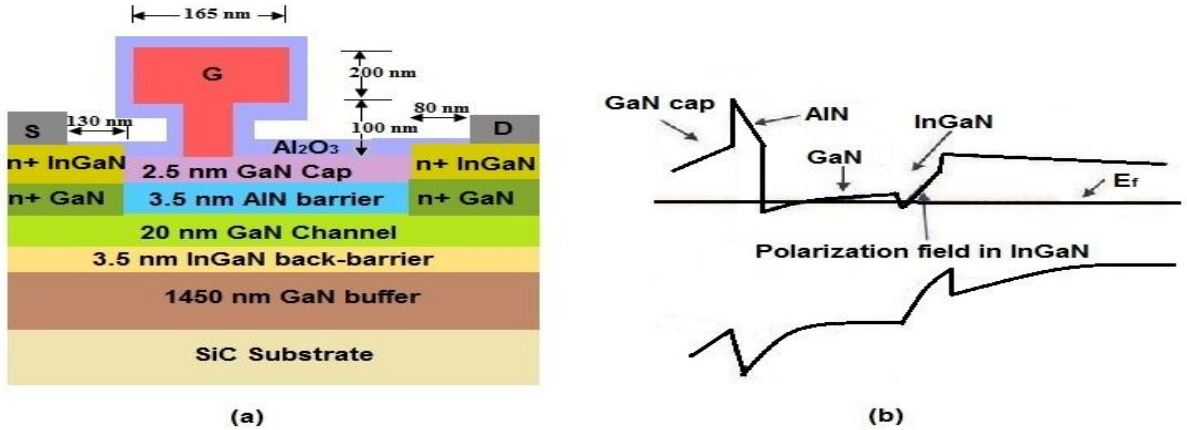

Figure 1.a) Vertical cross-section of AlN/GaN/InGaN Heterostructure b) Energy band diagram

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The vertical cross section of AlN/GaN HEMT device structure is depicted in Fig.1. The device consists of SiC substrate to achieve good thermal stability, 1450 nm Fe doped GaN buffer layer which isolate the channel from the substrate defects, 3.5 nm InGaN back-barrier layer which helps to confine the more electron in the channel due its effective conduction band notch at the interface with GaN channel and also it contributed for higher carrier mobility in the 2DEG (~1500 $cm^2/V\text{-}s$). Moreover the buffer leakage current is suppressed by the InGaN back-barrier. The channel region is defined by 20 nm GaN and 3.5 nm AlN is used as barrier layer. The induced spontaneous and piezoelectric polarization electric field provides an improved sheet charge carrier density of 1.9 $\times 10^{13}$ cm^{-2} in the 2DEG and also due to the higher band gap of the barrier limits the gate leakage current and mitigates the short channel effects in the device. The source and drain regions are formed by heavily doped n+ GaN/InGaN with Si in the order of ~ 7×10^{20} cm^{-3} to minimize the contact resistances. The source and drain ohmic contacts were designed by using Ti/Pt/Au metal stack and T shaped gate is formed by Pt/Au metal stack. T-gate structure with stem height of 100 nm with 20 nm footprint is designed, which liftoff wide cross sectional gate area with smaller gate length and Schottky contact is formed by Ni/Pt/Au metal stack. The drain to source separation is kept at 110 nm. In order to reduce the parasitic capacitances of the device, finally the device surface is fully passivated by 10 nm Al_2O_3 layer which greatly helped for achieving higher cut-off frequencies. Usually Si_3N_4 is the commonly used passivation layer to avoid the current collapses, but the larger thickness of passivation layer is needed, which will increases the gate capacitance particularly gate-drain capacitance (C_{gd}). In this model a 10 nm Al_2O_3 is used as passivation layer which assists to unfasten the dispersion effects and it provides a root to good transport property in the 2DEG [19].

The Conduction band offset diagram of AlN/GaN/InGaN is depicted in Fig.1.b. Due to induced piezoelectric polarization between InGaN and GaN there will be a sharp raised potential barrier is formed at the back of 2DEG channel. Such a sharp notch helps to confine the electron in better manner in the channel region and also it mitigates the buffer leakage current.

3. DRAIN CURRENT CHARACTERISTICS

In this work we investigated the DC and microwave characteristics of depletion mode HEMT for 20 nm gate length (Lg) and gate width of (w) of 2×40 µm AlN/GaN with InGaN back-barrier.

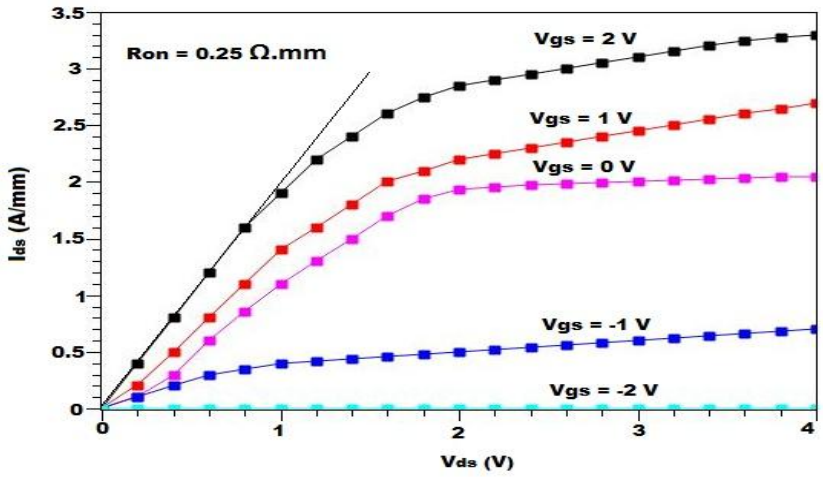

Figure 2. TCAD Simulation of Drain current Characteristics of 20 nm gate length AlN/GaN HEMT

Fig.2. is showing the V-I characteristics of Lg 20 nm, w = 2×40 µm D-mode AlN/GaN HEMT. The D-mode HEMT simulation result gives a peak current density of 3.3 A/mm at V_{gs} = 2 V and the device is pinched off perfectly at V_{gs} = -2 V.

The on resistance (R_{on}) of the transistor is the primary source for power dissipation when the operation in active the region. The extracted very low on resistance (R_{on}) of the proposed device at V_{gs} = 2 V is 0.25 Ω.mm.

This higher current density is achieved mainly because of the enhanced carrier mobility with greater sheet charge carrier density in 2DEG channel. The wide bandgap (6.2 eV) AlN barrier provides effective conduction band offset and it reduces strain induced surface defects at the interface. Moreover, the InGaN notch helps to provide the better confinement of charge carrier in channel and also it suppressed the buffer leakage current in the device.

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The breakdown voltage GaN-based HEMT is the primary advantages for high power applications. However, scaling the gate length of HEMTs below 100 nm will lead to significant reduction in breakdown voltage due to high leakage currents. The breakdown characteristics of the proposed HEMTs by constant drain current injection method is displaying in Fig.3 for D-mode HEMT. In the proposed AlN/GaN HEMT structure, the gate leakage current and buffer leakage currents are majorly reduced with help of wideband gap barrier (AlN) and back-barrier (InGaN). The off-state breakdown voltage (V_{DS}) of 21 V extracted from the breakdown characteristics for I_d = 10 mA/mm. For 20 nm AlN/GaN HEMT, the obtained V_{BR} is the best result among the literature.

The transfer characteristic of D-mode HEMT is shown in Fig.4. for different drain-source bias (V_{ds}). The extracted threshold voltages of the device from the plot is -1.44 V

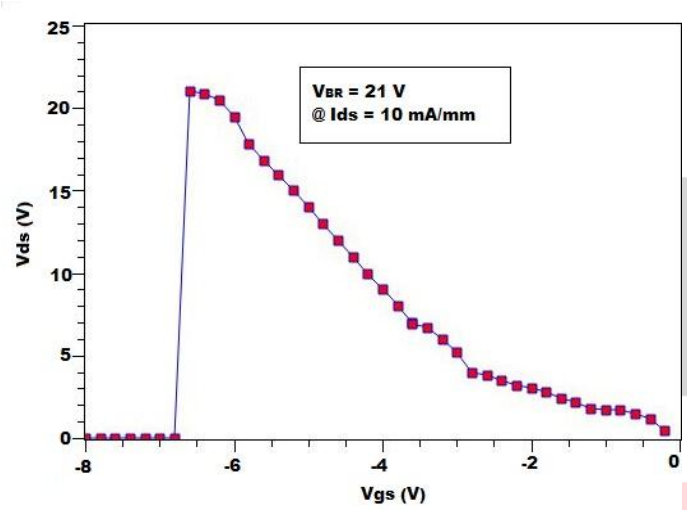

Figure 3. TCAD simulation of V_{ds} – V_{gs} breakdown characteristics of 20 nm gate length D-mode AlN/GaN HEMT with InGaN back-barrier

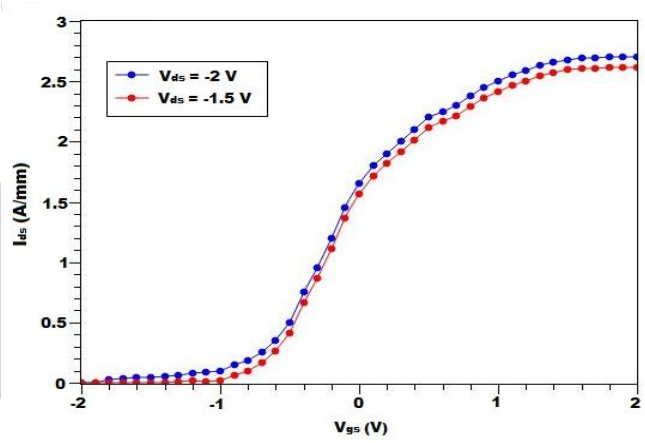

Figure 4. Transfer Characteristics of of 20 nm gate length AlN/GaN HEMT

4. SUBTHRESHOLD AND LEAKAGE CURRENT CHARACTERISTICS

The Gate leakage current of the HEMT is comprises of surface leakage and barrier leakage currents. 1. The electrons tunnelling from the gate accumulates on the GaN (cap layer) surface next to the gate and then conducts along the surface states by a trap-to-trap hopping mechanism. 2. Poole-Frenkel (PF) emission creates the gate to drain surface leakage current. At the low electric field hopping conduction is the main mechanism of surface leakage and for high electric field PF emission would be the main source for surface electron transportation. The electron at the gate side can travel through the AlN barrier layer to the 2DEG channel, resulting in the barrier leakage current. The barrier leakage current includes thermionic emission (TE), Fowler-Nordheim (FN) tunnelling, PF emission and other trap assisted emission. The FN tunnelling process is independent of temperature, but strongly depends on electric field. Because of the large electric field resulting from the high spontaneous polarization charge, FN tunnelling current becomes one of the dominant leakage current in AlN/GaN HEMTs. PF emission and other trap assisted emission can be depressed by improving the material quality.

FN tunneling current density $J_{FN} = AE^2 e^{\left[\frac{-B}{E}\right]}$ (2)

With $= \frac{8\pi\sqrt{2m_n^*(q\varphi_{eff})^3}}{3qh}$. Where E is the electric field in the barrier at the metal-semiconductor interface, A is the constant, m_n^* is the conduction band effective mass in semiconductor, h is the Planck's constant and φ_{eff} is the effective barrier height. In this work, the Fowler-Nordheim (FN) tunnelling gate leakage current characteristics of the proposed HEMT are simulated by Synopsys Sentaurus TCAD Drift-Diffusion transport model.

The gate leakage current characteristics of Lg 20 nm AlN/GaN HEMT with InGaN back-barrier is shown in Fig.5. For high voltage switching applications reverse bias gate leakage current is a series problem affecting the device performance. The wide band gap (6.01 eV) AlN barrier not only reducing the alloy scattering, which also effectively

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reduces the Fowler-Nordheim (FM) tunneling current at high reverse gate voltages. At zero gate bias, the gate leakage current (I_g) for depletion mode HEMT is ~10^{-13} A/mm.

The short channel effects are the major problem in ultra-scaled devices, particularly in sub 50 nm gate lengths. The inclusion of InGaN back-barrier material in AlN/GaN HEMT reduces the short channel effects. The subthreshold characteristics of D-mode Lg 20 nm AlN/GaN with InGaN back-barrier is depicted in Fig.6. The extracted drain induced barrier lowering (DIBL) and subthreshold slope (SS) from the log scale plot are 112 mV/V & 81 mV/dec respectively.

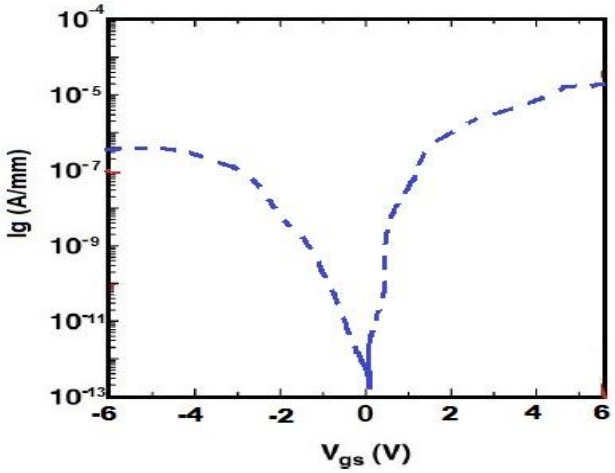

Figure 5. TCAD simulation of Gate Leakage current characteristics of of 20 nm gate length AlN/GaN HEMT.

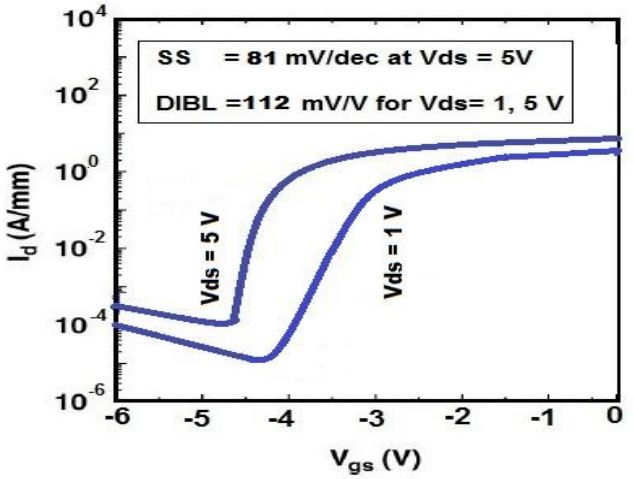

Figure 6. TCAD Simulation of Subthreshold characteristics of 20 nm gate length AlN/GaN HEMT

5. RF Characteristics of InAlN/GaN HEMT with AlGaN back-barrier

Fig.7. is displaying the transconductance variation with the gate-source bias voltage. The obtained peak extrinsic transconductance of the D-mode HEMT is 1.45 S/mm at V_{ds} = 2 V.

The current gain cut-off frequency (f_t) of HEMTs can be expressed as a sum of intrinsic and parasitic components [20];

$$\tau = \frac{1}{2\pi f_t} = \frac{C_{gs}+C_{gd}}{g_m} + C_{gd}.(R_s + R_d).\left[1 + \left(1 + \frac{C_{gs}}{C_{gd}}\right)\frac{g_d}{g_m}\right] \quad (3)$$

$$f_{max} = \frac{f_t}{2\sqrt{(R_s+R_g)g_{ds}+2\pi f_t R_g C_{gd}}}$$

Where C_{gs}, C_{gd}, g_m, g_d ,R_s, R_g and R_d represents gate-source capacitance, gate to drain capacitance, transconductance, drain conductance, source resistance, gate resistance and drain resistance respectively. The intrinsic transit time of the HEMT is $\frac{C_{gs}+C_{gd}}{g_m}$ and the parasitic charging time delay represented by $C_{gd}.(R_s + R_d)$ and the last term in the equation (3) is the delay originating from output conductance.

The simulation result of current gain cut-off frequency (f_t) and power gain cut-off frequency (f_{max}) of Lg 20 nm AlN/GaN HEMT with InGaN back-barrier of D-mode HEMT for various gate-source bias are extracted from the TCAD simulation and depicted in Fig.8. The proposed HEMT device exhibited a peak f_t/f_{max} = 451/448 GHz. The Johnson figure of merit (JFoM) of D-mode 9.471 THz-V.

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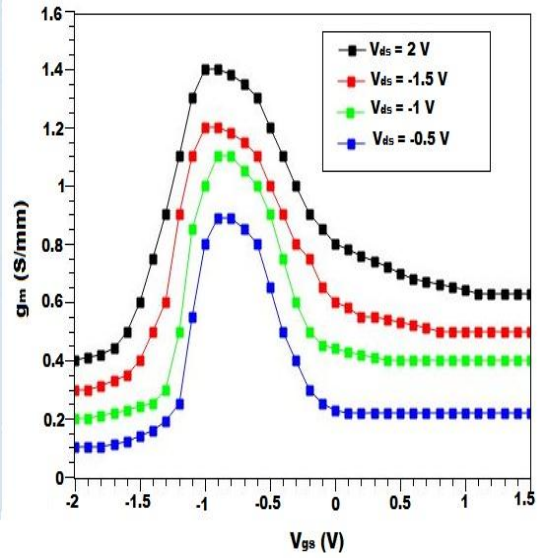

Figure 7. TCAD simulation of Transconductance variation with gate-source bias of 20 nm gate length AlN/GaN HEMT

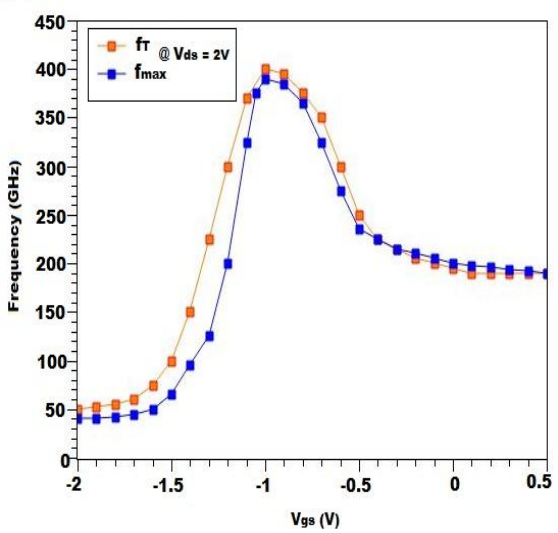

Figure 8. TCAD simulation of microwave characteristics of of 20 nm gate length AlN/GaN HEMT

The higher f_t/f_{max} are achieved by smaller gate length, the drastic reduction in the contacts resistances and the parasitic capacitances of the device by heavily doped (n+ GaN/InGaN) source/drain regions have direct contacts with the channel, combined Al_2O_3 passivated device surface. The features of the T-gate structure is reduced gate resistances & capacitances, short channel effects (SCEs), which improves the transconductance (g_m) and attenuated drain conductance. The extracted small signal parameters are gate-source capacitance C_{gs} , gate-drain capacitance C_{gd} , source resistance R_s , drain resistance R_d , Sheet resistance R_{sh} and on resistance R_{on} of the 20 nm T-gate D-mode AlN/GaN HEMT device with heavily doped source and regions are 312 fF/mm, 107 fF/mm, 0.37 Ω.mm, 0.12 Ω.mm, 435 Ω/□ and 0.25 Ω.mm respectively.

Parameters used for TCAD simulation (at room temperature)

The various parameters used for TCAD simulation for this work is listed in Table 1.

Table 1. List of parameters for TCAD simulation

$\Delta E_{C_{InAlN/GaN}}$	$0.8\ eV$	ε_{InAlN}	10.1
$\Delta E_{C,AlN/GaN}$	$1.7\ eV$	ε_{AlN}	8.57
$\sigma_{InAlN/AlN}$	$-3.57X10^{13}Cm^{-2}$	ε_{AlN}	9.5
$\sigma_{AlN/GaN}$	$6.64X10^{13}Cm^{-2}$	$\emptyset_s$	2.8 eV
m_{InAlN}	$0.25m_o$	AIN_χ	2.1 eV
m_{AlN}	$0.32m_o$	$InAlN_\chi$	2.5 eV
m_{GaN}	$0.20m_o$	InN_χ	4.7 eV

Where,

ΔE_c - Conduction band offset

σ - Polarization induced interface charges

ε - Static dielectric constant

$\emptyset_s$ - Surface potential

m - Electron effective mass

x - electron affinity

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6. CONCLUSION

In this work, the DC and microwave characteristics of a novel 20 nm T-gate AlN/GaN HEMT with InGaN back-barrier has been demonstrated by using Synopsys TCAD tool. The device features are heavily doped n+ InGaN/GaN source and drain regions with Al_2O_3 passivated device surface which is helped us to reduce the contact resistances and gate capacitances of the device which uplift the microwave characteristics of the HEMTs. 20 nm gate length D-mode HEMT exhibited a peak drain current density I_{dmax} of 3.3 A/mm, transconductance g_m of 1.45 S/mm, current gain cut-off frequency f_t of 451 GHz and power gain cut-off frequency f_{max} of 448 GHz. The three terminal off-state breakdown voltages of 21 V is achieved for D-mode HEMT. The excellent microwave characteristics with the higher breakdown voltage of the proposed GaN-based HEMT are the expected to be the most optimistic applicant for future high power millimeter wave electronics.

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