An Advanced Modified Cascaded Switch-Ladder Multilevel Inverter Structure

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***Abstract*— An Advanced Modified Cascaded Switch-Ladder Multilevel Inverter Structure is presented and it generates an optimum number of voltage output levels. Firstly, a fundamental switch-ladder multilevel structure is described. Then, the structure of recommended cascaded topology based on series connection of fundamental switch ladder topologies is presented. To generate optimum number of levels with minimum number of switching elements, dc sources and voltage on switches, the proposed cascade topology is modified for better results. After a detailed evaluation of the results, it is proven that the proposed cascaded topology involves lesser number of components. In addition to that the value of voltage rating on switches is lesser compared to existing system. Test outcomes for two topologies are analysed to verify the performance of proposed topology. Matlab simulink model is used to evaluate the performance of cascaded switch-ladder multi level inverter topology.**

Keywords: Multilevel Inverter Operation, Optimization, Cascaded switch-Ladder, Voltage level.

I. INTRODUCTION

Multilevel inverters have several applications. These devices are cost effective. As technology advances at a faster rate, it is not possible to avoid the usage of power conditioning devices. Since multilevel inverters are used in lot of scenarios, it is the rule of thumb to enhance the structure of these devices with regard to bringing down in numbers the components and voltage rating ion switches. Some of the conventional Multi level inverters are the cascaded H-bridge inverter(CHB) , the neutral-point-clamped inverters and flying capacitors. Flying capacitor inverters provide switch combination redundancy for balancing different voltage levels. Both real and reactive power flow can be controlled. These broadly studied and readily available Multilevel inverters are instrumental in aiding for high-quality ac supplies and motor drivers in industrial application due to their good performance. The duty cycle of both switches is controlled in such a way that in one input, multi-output DC-AC inverters the voltage on all output capacitors are adjusted to same voltages. Lower total harmonic distortion(THD) is needed in high voltage induction motor drives. In the existing system, 13 levels were used in the multi level inverter. In the proposed system, 15 levels are used. One switch has been added as compared to existing system. Source levels are even. In the existing system, input voltage is 1-1-2-2. In the proposed system, the input voltage has been changed as 1-1-2-3. 15 levels are output.

II. RELATED WORKS

This chapter briefly discusses the development of non linear transcendental Selective Harmonic Elimination (SHE) equation problem in control of multilevel inverter with an objective of controlling the chosen multilevel inverter configuration during whole range of modulation index from 0 to 1 with less %THD which complies with IEEE 519-1992 harmonic guidelines and also with less switching losses. Commercially existing topologies of multilevel inverters and modulation strategy for the control of multilevel inverters are briefly reviewed. It also reviewed the research progress of various techniques for solving non linear transcendental SHE equation problem. This chapter also presents the objective of research, research methodology and the thesis organization.

A BRIEF REVIEW OF MULTILEVEL INVERTER TOPOLOGIES

Now-a-days, power requirements of modern industries have reached to megawatt level. In particular, high-power medium voltage drives requires power in megawatt range and is usually connected to the medium voltage network. It is troublesome to connect a single power semiconductor switch directly to medium voltage grid (2.3kV,3.3kV, 4.16kV or 6.9 kV). For this reasons, multilevel inverter have emerged as a cost effective solution for high voltage and high power applications including power quality and motor drive problems [26]. As a cost effective solution, multilevel converter not only achieves higher voltage and current ratings, but also enables the use of low power application in renewable energy sources. These converters are suitable in high voltage and high power applications due to their ability to synthesize higher voltages with a limited maximum device rating, less harmonic distortion,

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producing of smaller common-mode voltage (CM), less electromagnetic compatibility (EMC) problems and attain higher voltage with a limited maximum device rating.At present, multilevel inverters are extensively used in various applications such as HVDC transmission [27], distribution generation systems[28], medium voltage motor drives[29], Flexible AC Transmission System (FACTS) , traction drive systems , var compensation and stability enhancement, active filtering, chemical, liquefied natural gas (LNG) plants, marine propulsion, electric vehicle systems (EVS), hybrid electric vehicle systems(HEV) and adjustable speed drives. The range of the output power is a very important and evident limitation of two-level inverter. However, this problem can be overcome by introducing the concept of multilevel converters in 1975. The concept of multilevel began with the three-level converter which is often known as neutral-point converter (NPC) . The word "converter" refers to the power flow in both the directions i.e. from ac to dc called as "rectifier" and from dc to ac called as "inverter". The word "multilevel inverter" refers to using a multilevel converter in the inverting mode of operation. In order to meet the challenges such as high dv/dt causing voltage doubling effect in motor output voltage waveform, %THD to comply with IEEE 519-1992 harmonic guidelines, high electromagnetic interference (EMI), high common-mode voltages and requirements of synthesizing higher voltages for modern industrial applications have subsequently led the development of various inverter topologies. The commercially existing inverter topologies are neutral point clamped (NPC) inverter, flying capacitor (FC) and cascaded H-bridge (CHB) inverter topologies and are briefly reviewed in next section.

Neutral-Point Clamped (NPC) or Diode-Clamped Topology

One of the traditionally accepted and widely used topology for various industrial and power sector applications is neutral point converter which was proposed by Nabae, Takahashi and Akagi in 981. As the two-level inverter has the drawback of achieving higher power levels with the available GTOs of 4.5kV voltage rating at that time, for traction applications, three-level inverter configuration was developed to meet the requirement of high voltage dc operation in traction application in Austrian railways. Three-level neutral point converter often called as three-level diode-clamped inverter has found wide range application because of the advantages such as higher power handling capability, less dv/dt and less %THD when compared to conventional two-level inverter. Later, direct extensions of the original NPC for higher number of levels are presented by several researchers in 1990s and presented experimental results for the applications such as variable motor drives, static var compensation and medium voltage systems interconnections. The diode-clamped multilevel inverter employs clamping diodes and cascaded dc capacitors to produce ac voltage waveforms with multiple levels. However, as the number of levels has increased the number of clamping diodes, switching devices and dc capacitors also increases, thus the circuit configuration becomes more complicated. In general, for an *m*-level diode clamped inverter, for each leg *2(m-1)* switching devices, *(m-1) * (m-2)* clamping diodes and *(m-1)* dc link capacitors are required. In NPC topology, number of blocking diodes is quadratically related to the number of levels in the output voltage waveform. However, by increasing the number of voltage levels the quality of the output voltage has improved and the voltage waveform becomes closer to sinusoidal waveform. This means that for an *m*-level diode-clamped inverter has an *m*-levels in output phase voltage and a *(2m-1)* - levels in output line voltage waveform. The diode D_{a2} represented in Fig. 2.1 requires two diodes in series because it blocks two capacitor voltages, and the diode $D_{a(m-2)}$ requires *(m-2)* series-connected diodes because it blocks (*m*-2) capacitor voltages.

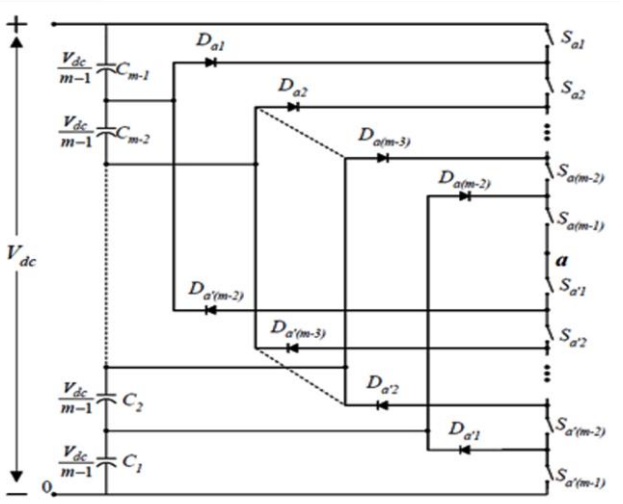

Fig: 2.1 An *m*-level Neutral Point Clamped inverter topology

Generally, the voltage across each capacitor for an *m*-level diode clamped inverter at steady state is *Vdc/(m-1),* where *Vdc* is dc bus voltage. Though, switching devices in NPC topology are required to block only a voltage level of *Vdc* but the clamping diodes require different ratings to block the reverse voltage. As the number of levels has increased the capacitor voltage balancing becomes a major problem.

III. PROPOSED SYSTEM

The input voltage level of the proposed basic unit is indicated in Fig. below. It presents novel cascaded multilevel inverters that can solve the total harmonic distortion reduction. By using a cascaded topology based on parallel connection of H bridge. The output voltage of CSLMI(V_{out}) is equal to the sum of output voltage of the all FSLMI. The maximum voltage rating on a switch is an important parameter which affects the inverter cost. Total

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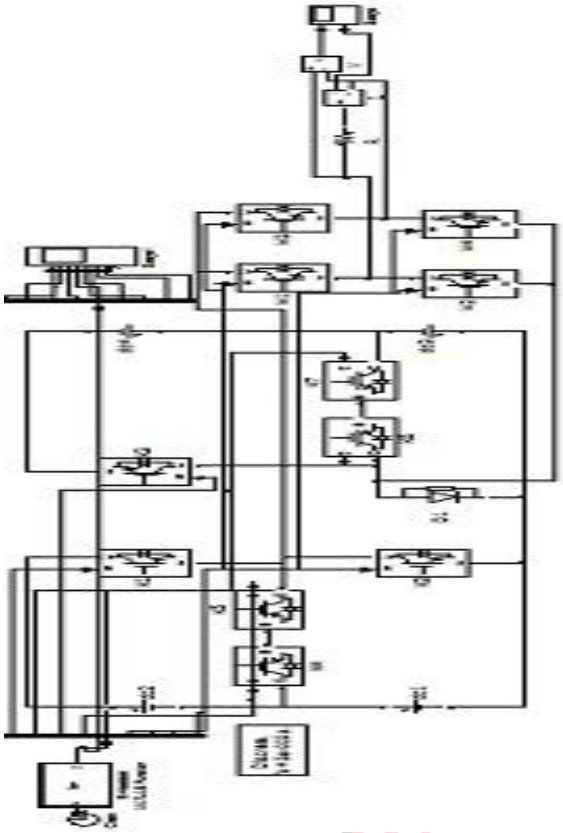
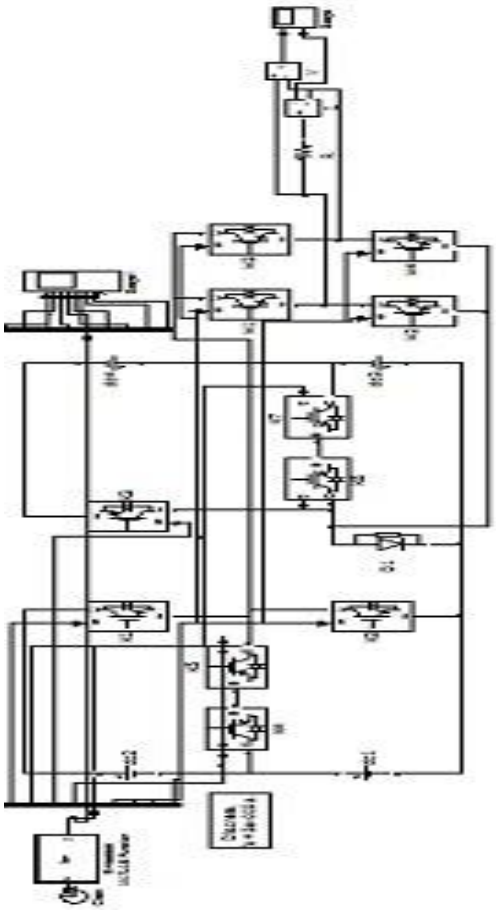
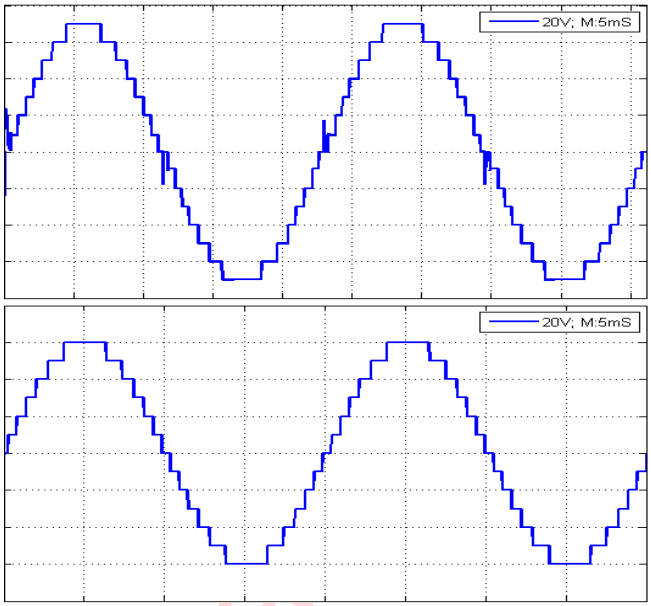
maximum voltage rating on unidirectional and bidirectional switches respectively are optimum level.



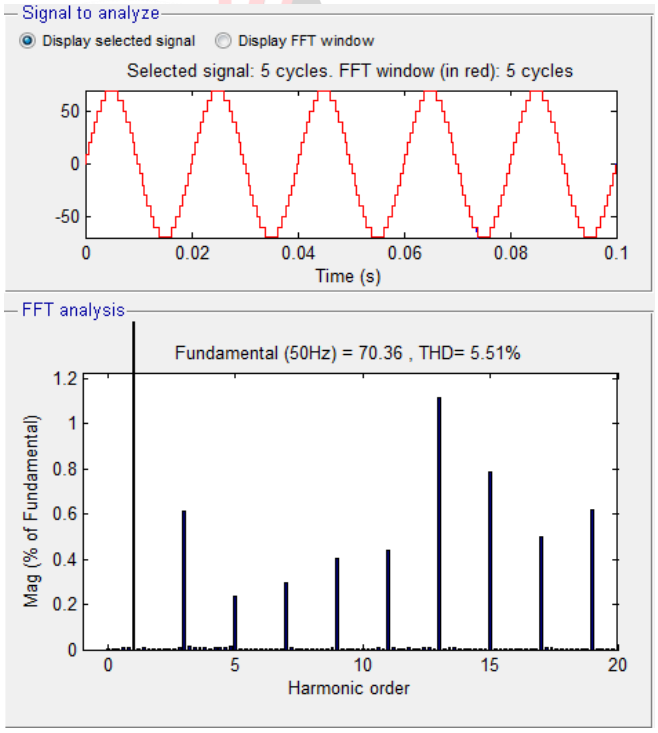


Therefore, the proposed CSLMI topology can be used in high voltage applications. The current rating of switches is another important parameter in the design of a converter. In the proposed topology, when the switches are turned off, the current tend to be zero. However, when the switches are turned on , the maximum current of the switches are equal to the load current.

IV.OUTPUT WAVEFORMS AND FFT ANALYSIS



The signal to analyze has been shown underneath. The selected signal involves 5 cycles.



V.CONCLUSION

In this project, performance improvement of modified cascaded switch-ladder multi level inverter was described in this paper. The presented cascaded topology was optimized due to the extended feature of proposed topology. The main aim of optimization was generating maximum number of power electronics components and voltage rating on switches. Moreover, a good

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approximation for the average power loss in the active and passive switches is given in simple expressions in terms of current, amplitude depth and power factor for typical conditions prevailing in CSLMI inverters.The results of comparisons indicated that the proposed cascaded topology could overcome the disadvantages of other structures.

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