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Studies on Electrical Properties of $(Ta_2O_5)_{87.5}$ and $(TiO_2)_{12.5}$ Mix Oxide for MOSFET

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Abstract - The scaling down of CMOS transistor requires replacement of conventional silicon dioxide (SiO_2) layer with high K material for gate. In this current work mixed oxide of $(Ta_2O_5)_{87.5}$ and $(TiO_2)_{12.5}$ is chosen as alternative to SiO_2. Capacitance, Fixed charges, Interface state density and Leakage current of that film is calculated. P-type single crystal silicon <100> is selected as substrate and DC reactive magnetron sputtering method with combination of Ta and Ti metal targets to deposit thin film. Oxygen is used as reactive gas along with Argon. The thickness of deposited film is in the range of 300±10 nm with substrate temperature 600^0C. Agilent make 4284 A L-C-R meter along with Karlsuss wafer probe station is used for C-V measurement and Agilent 4155 model is used for I-V measurement. MOS capacitor has been fabricated with Aluminium as top electrode to perform bi-directional CV and IV analysis. Flat band voltage (V_{FB}), Fixed charges (Q_f), Interface state density (Dit') and Equivalent Oxide Thickness (EOT) are obtained from the bidirectional C-V analysis. The maximum dielectric constant achieved for MOS structure is 34.28 when Titanium is 12.5% and Tantalum is 87.5%.

Keywords —Capacitance, Sputtering, thin film, Fixed charges, Interface state density, Leakage current

I. INTRODUCTION

The success of the semiconductor industry relies on the continuous improvement of integrated circuit performance. This improvement is achieved by reducing the dimensions of the key component of the circuit like MOSFET [1] [2]. The scaling of MOSFET was easily accomplished using SiO_2 as gate oxide layer but fundamental limit is the exponential increase of direct tunneling current as function of the SiO_2 thickness [12]. The concept of High-K replace is to reduce direct tunneling, and make the physical thickness of the gate dielectric larger, but keep the capacitance the same as an equivalent SiO_2 film. The requirement for the successful implementation of new high dielectric constant gate oxide materials in MOSFET application need to be fully understood before these materials can be adopted by industry [13]. The gate dielectric is used to isolate the gate terminal from the current carrying channel region. The dielectric material must be an insulator with a band gap greater than 5eV and there is an inverse relationship between dielectric constant and band gap. A closely related property is the height of the potential barrier presented to tunneling electrons from the conduction band and to tunneling holes from the valence band. Interface preparation and quality is important from layer growth point of view as well as performance point of view. There is inverse correlation exists between the thickness and quality of the interfacial layer and charge carrier mobility especially for electrons. There should be low interface trap density. The oxides must have a large Gibbs free energy of formation to prevent reaction with silicon. Oxygen diffusion coefficients must be low as they will cause uncontrolled interfacial layer regrowth [14] [15]. Hence, this interface must be of the highest electrical quality, in terms of roughness and the absence of interface defects [11].

Ta_2O_5, also known as tantalum oxide is a high –dielectric constant (26-50) material with reasonably low leakage current ($1*10^{-8}$A/cm^2 at 1 V) and high breakdown strength (5-6 MV/cm). It exists in both orthorhombic and hexagonal phases also known as low and high temperature forms. The low temperature form is known as β-Ta_2O_5, and the high temperature form is known as α-Ta_2O_5. The transition point between these two forms has been reported as 1360°C. The transition is slow but reversible. The structures of both forms consist of chains built from octahedral and pentagonal bipyramidal polyhedra sharing opposite vertices. These chains are further joined by sharing edges to yield the 3D structure. Although the dielectric constant of Ta_2O_5 is lower than other oxide films such as $SrTiO_3$, $Ba_xSr_{1-x}TiO_3$, $Pb_xZr_{1-x}TiO_3$ but Ta_2O_5 can be deposited by PVD and CVD which is suitable for mass production. Excellent step coverage characteristic can be obtained by number of methods compatible with Si technology. One of the advantages of Ta_2O_5 is by relevant annealing it is possible to improve the film stoichometry to make more abrupt interfaces to reduce structural non perfections and by this way to control and maximize dielectric. The higher K comes at the expense of a smaller band gap and lower conduction and valence band offsets between Si and Ta_2O_5. The band gap of Ta_2O_5 is 4.5 [9] at the same time it has low

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leakage current indicating that it has fewer problems than other materials.

TiO_2 also known as titanium oxide occurs in nature as minerals rutile, anatase and brookite, and additionally as two high pressure forms, a monoclinic and an orthorhombic form, TiO_2 has high permittivity (30 for Anatase phase and 80 for Rutile phase) and also it has appreciable conduction band offset of 1.2 eV with Silicon.

II. EXPRIMENTAL

A. Experiment

All the experimental work is aimed at the preparation of mixed oxide $(Ta_2O_5)_{87.5}$ and $(TiO_2)_{12.5}$ thin film and to study the effect of process parameters and also the electrical properties of the prepared films [12].The substrate material used for the deposition of mixed oxide $(Ta_2O_5)_{87.5}$ and $(TiO_2)_{12.5}$ films is P– type single crystal silicon with <100> orientation having a doping concentration of 0.2 x 10^{15} to 2.2 x10^{15} cm^{-3} boron atoms (according to the doping information provided by the manufacturer).The 4″ wafers are cut down into small pieces of rectangular/square shape before depositing the mixed oxide $(Ta_2O_5)_{87.5}$ and $(TiO_2)_{12.5}$ thin film[8]. For MOS configuration Aluminium electrodes were deposited on the dielectric film using a mechanical mask. Aluminium electrodes have been deposited using thermal evaporation process. First the samples are subjected to ultrasonication for removing the contaminants like dust particles then cleaned in Piranha solution (a warm mixture of sulphuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) in 1:3 ratio) to remove any organic residues left on the substrate and to make it hydrophilic. Samples are rinsed in De Ionized (DI) water and then dipped in 5% HF solution to remove any native oxide (SiO_2) present on the samples. Finally the samples are rinsed in DI water and then flushed with dry air prior to loading in the deposition chamber.

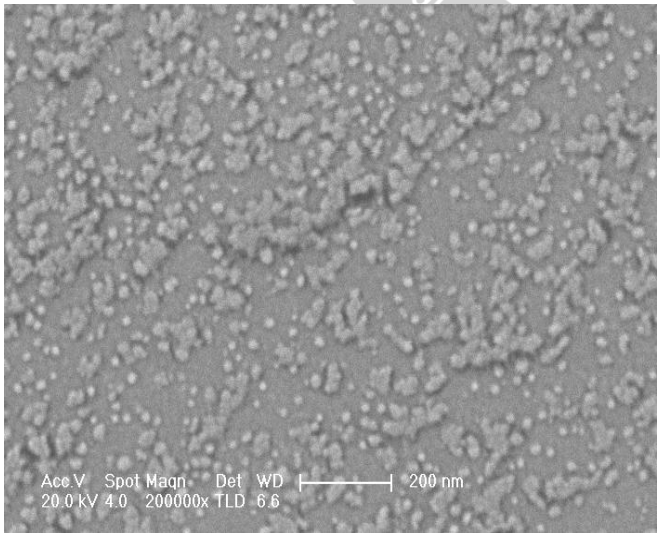

Fig.1 SEM image of mixed oxide film

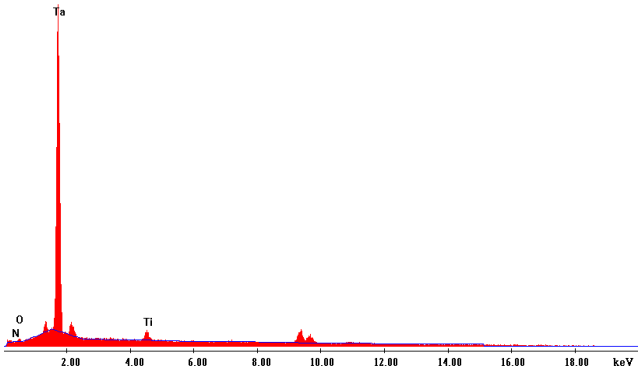

Fig.2 EDX image of mixed oxide film

The sputtering system used is a homemade deposition system, which is having a provision for the deposition of 3 materials. DC reactive magnetron sputtering has been used. The target material used is a Mosaic target, which is a combination of 3" diameter circular disc of Tantalum and small Titanium pieces having different areas. Argon (99.99% pure) and Oxygen (99.999% pure) are used as sputtering and reactive gas respectively. The sputtering chamber is evacuated to a base pressure of 1.0* 10^{-5} mbar using a diffusion pump and rotary pump combination. The partial pressures of the two gases have been controlled by using mass flow controllers. The substrate to target distance is 6 cm.

B. Deposition of Film

Before attempting the deposition of mixed oxide film, the process parameters have been optimized for deposition of Tantalum oxide films by depositing films at different current densities and different thicknesses at a base vacuum of 1.0*10^{-5} mbar, Oxygen partial pressure of 6*10^{-4} mbar and sputtering pressure of 4*10^{-3} mbar with substrate temperature of 600^{o}C [4]. Then select the optimized parameter to deposit mix oxide film of desired composition. The mosaic target has Ta and Ti metal with area 87.5% and 12.5% respectively as sputtering yield is same for both the metal we get the required mixed oxide $(Ta_2O_5)_{87.5}$ and $(TiO_2)_{12.5}$ thin film. The area of the device or MOS capacitor used is 13278.57*$10^{-10}$$m^2$. The metal contact used is aluminium. The topography of film is observed with SEM and the composition of the film is measured with EDX. The topography and the composition are as shown in fig.1, 2. From SEM and EDX results we checked that the film which we are getting is mixed oxide film with required element and composition. We measured the thickness of the films using profilometer. The thickness of prepared mixed oxide film is in the range of 300+-10 nm. Metal oxide semiconductor MOS Capacitor of mix-oxide $(Ta_2O_5)_{87.5}$ $(TiO_2)_{12.5}$ was prepared for the electrical studies.

For performing the Capacitance – Voltage measurements Agilent make 4284A L–C–R meter having operating frequency range from 20Hz to 1MHz is used along with a KarlSUSS make PM8 model probe station. Lab view

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program is used to interface L–C–R meter with a Computer in which data is collected and also plotted simultaneously [6].The options available in this program are setting the bias voltage range, probing signal frequency. The probe station is having a vacuum chuck to hold the sample firmly to avoid displacing of the sample while probing and also to provide proper electrical contact at the back side of the wafer. The tip of micro–manipulator is made of tungsten. The substrate doping concentration is obtained by measuring the minimum capacitance from the high frequency (1MHz) C–V curve of two samples for better comparison. The doping concentration of the p–type substrate is obtained as $4x10^{14}cm^{-3}$ boron atoms. Before performing the analysis of data from various samples, theoretical simulation for the C–V characteristics has been performed with a readily available MATLAB program. Various inputs provided to the program are thickness of the oxide film, metal–semiconductor work function difference value (Φms), substrate doping concentration (Na), area of the capacitor (A) and also the dielectric constant (K) [7].

For performing the bi directional Capacitance–Voltage scan on MOS capacitor an alternating voltage of 5mV amplitude is super imposed onto a DC voltage, which is swept from accumulation region to inversion region (i.e. from – voltage to + voltage) and again from inversion to accumulation. The range of the DC voltage as well as the DC voltage step value is varied between different samples to get the best possible curves. The bi directional C–V curves for the film with AC voltage = 5mV, frequency = 1MHz has studied. The bi directional C−V scan performed on film has a finite hysteresis and among the factors which cause the hysteresis in the bi directional C−V the fixed charges (either positive or negative) which are close to the oxide interface. We have observed both kinds of charges in our study and the magnitudes of the fixed charge densities are calculated. [10]

Interface Trapped Charge Density (Dit')

The interface trapped charge density has been measured using the analytical technique given by Jakubowski and Iniewski [5]. In this technique we need to find out the capacitance value from the corresponding high frequency C– V curve and we need to use the following formula to find out the amount of Dit' which has a unit of $cm^{-2}eV^{-1}$.

$$Dit' = Cmax\ (\Delta UG' - \Delta UG)/q^2 A \Phi F \quad cm^{-2}\ eV^{-1} \quad (1)$$

A =Area of the MOS capacitor
ΦF=Fermi potential of the P type Si
Cmax=Maximum Capacitance from C-V Graph
ΔU'G=Difference of the gate voltages corresponding to the surface potential of (1+ΦF/2) and (1+3ΦF/2).
ΔUG=Difference of the gate voltages corresponding to the surface potentials of (1+ΦF/2) and (1+3ΦF/2) calculated from the curve.

From calculation the interface state density is $20x10^{30}$ $cm^{-2}eV^{-1}$ for the deposited thin film .Interface state density is higher for thick film due to oxygen de passivation and defect generation at interface. The defects at the interface should be as low as possible.

Fixed Charge Density (Q_f)

Fixed charge is the inherent charge present with most of the oxides that may be thermally grown or deposited onto silicon. The fixed charge present in the oxide is found out from the shift in the flat band voltage value measured from the C–V curve and the analytical flat band voltage value[16]. In our work we found out that the fixed charge is negative. The fixed Oxide charge we got is $7.3x10^{11}cm^{-2}$.

Flat band Voltage (V_{FB}) & Threshold Voltage (V_{TH})

The V_{FB} is the most important parameter for a MOSFET because it is the factor that decides the V_{TH} and also the amount and polarity of the fixed charges present in the gate oxide. The V_{FB} observed for the sample is 0.2648 V and V_{TH} is 0.43 V.

Equivalent Oxide Thickness (EOT)

A number used to compare performance of high-k dielectric MOS gates with performance of SiO_2 based MOS gates. It shows thickness of SiO_2 gate oxide needed to obtain the same gate capacitance as the one obtained with thicker than SiO_2 dielectric featuring higher dielectric constant. The EOT observed for sample is 33.8nm.

Current–Voltage (I–V) Analysis

For performing the I–V analysis we used Agilent 4155 .The minimum leakage current density achieved is $3.5x10^{-7}A/cm^2$. The breakdown voltage considered above 45V corresponding to the field of 1.5 MV/cm. The leakage current is minimum and the breakdown voltage is high for film of 300nm.

III. CONCLUSION

Further scaling of MOSFET requires high k dielectric material. $(Ta_2O_5)_{87.5}$ and $(TiO_2)_{12.5}$ mixed oxide thin film obtain from DC reactive magnetron sputtering and annealing with 600^0C is chosen. Detail electrical properties for MOS structure for that thin film has been studied. Annealing process shows effect on quality of the grown oxides and their interface with Si which is a direct result of the oxidation temperature. The fixed charge for that film is $7.3x10^{11}cm^{-2}$.The interface state density is $20x10^{30}$ $cm^{-2}eV^{-1}$ and EOT that achieved is 33.8 nm. From the I-V analysis the minimum leakage current density achieved is $3.5x10^{-7}A/cm^2$. The deposition of Ti into Ta_2O_5 causes generation of negative oxide charge which reduces the existing positive charge in Ta_2O_5 and that result in decrease of leakage current. The breakdown voltage is at 45V

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corresponding to the field of 1.5 MV per cm. The high dielectric constant, low leakage current, high break down voltage, low interface trap charged density indicate that $(Ta_2O_5)_{87.5}$ and $(TiO_2)_{12.5}$ thin film are encouraging for the possibility of gate oxide layer for microelectronic applications.

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